**ECE 429 Lab 7**

**Carry-Ripple Addition II**

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**Introduction**

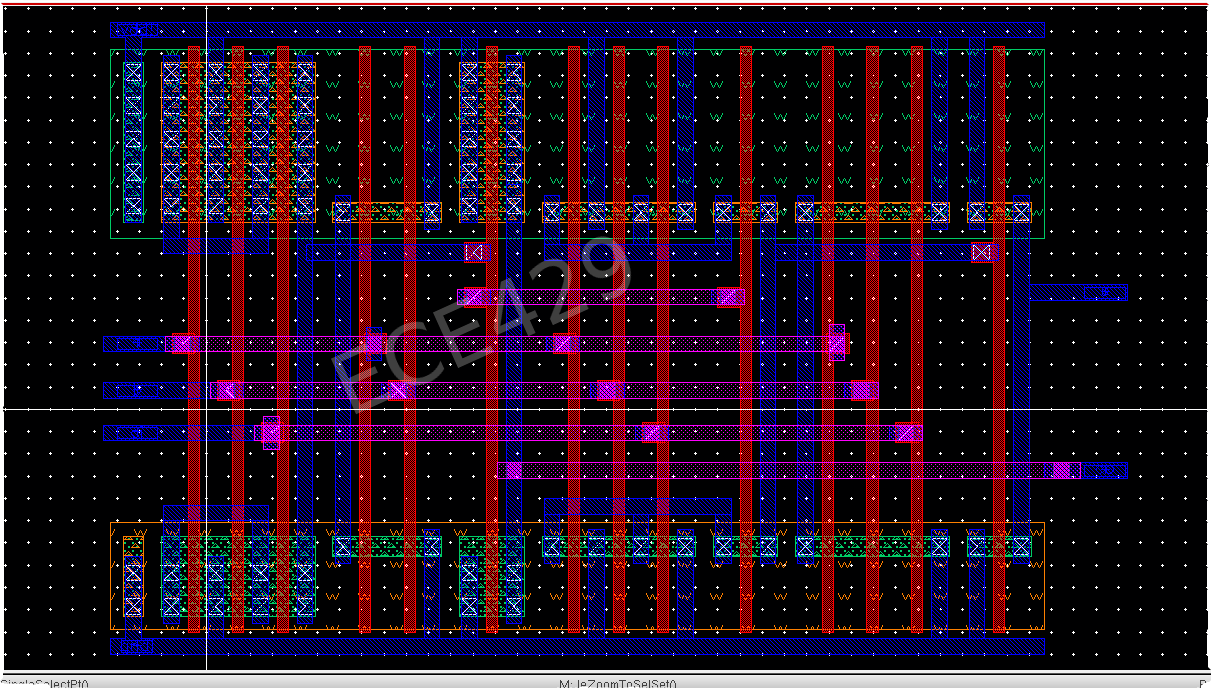
The objective of this lab is to design a layout for a full adder, like the one that was designed in lab 6. This layout, along with the adder schematic, will be used to build a 4-bit adder in lab 8.

**Theory/Pre-Lab**

The theory for this lab is the same as the previous lab. This time, a layout will be designed. It can be a long and tedious process, and a DRC must be run periodically to ensure the layout design follows the rules. Once the design is complete, a LVS check will verify that the layout performs as it should.

Although a stick diagram should have been made, I decided to use the example layout provided.

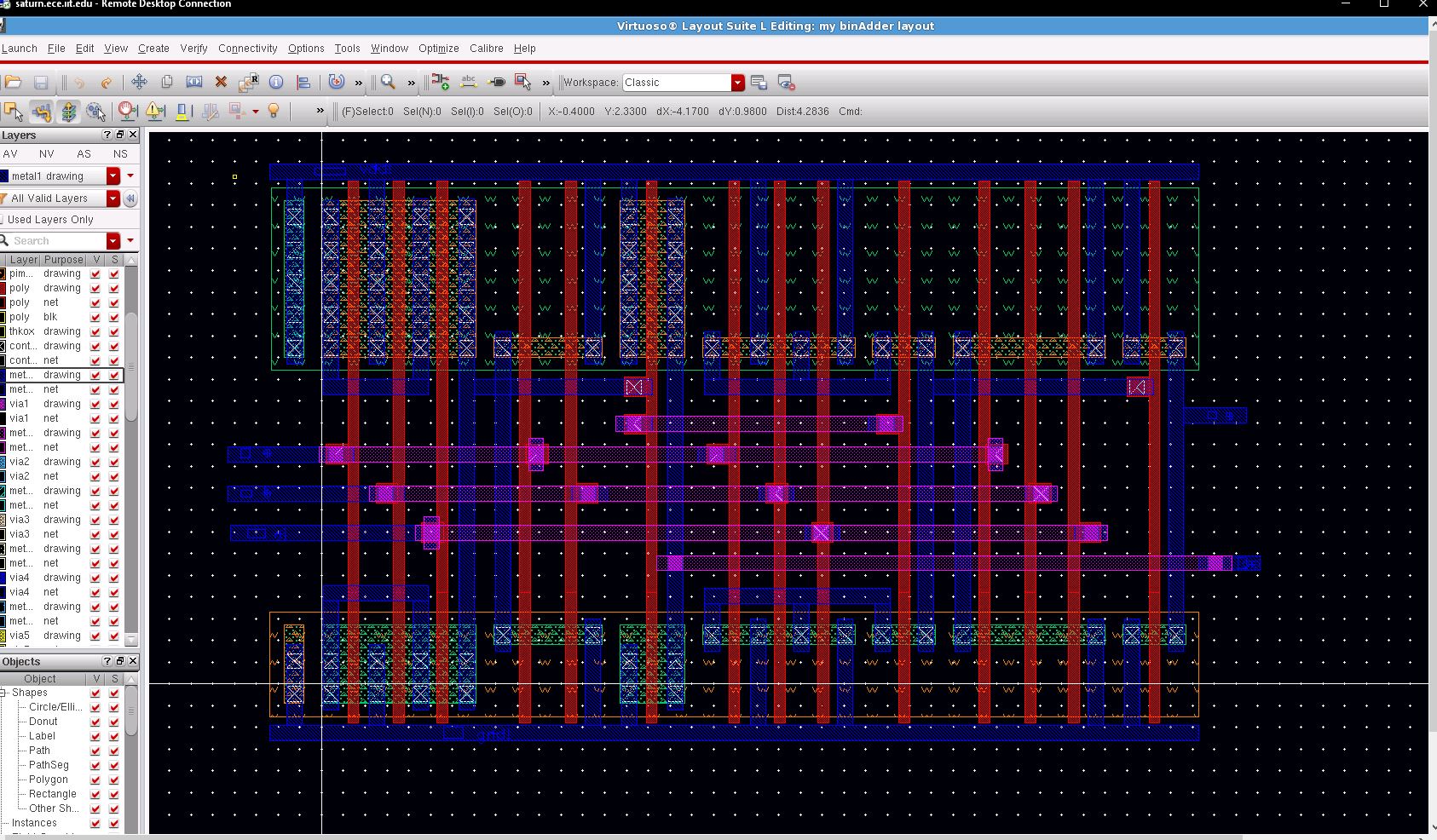
**Figure 1: Example Adder Layout**

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**Implementation**

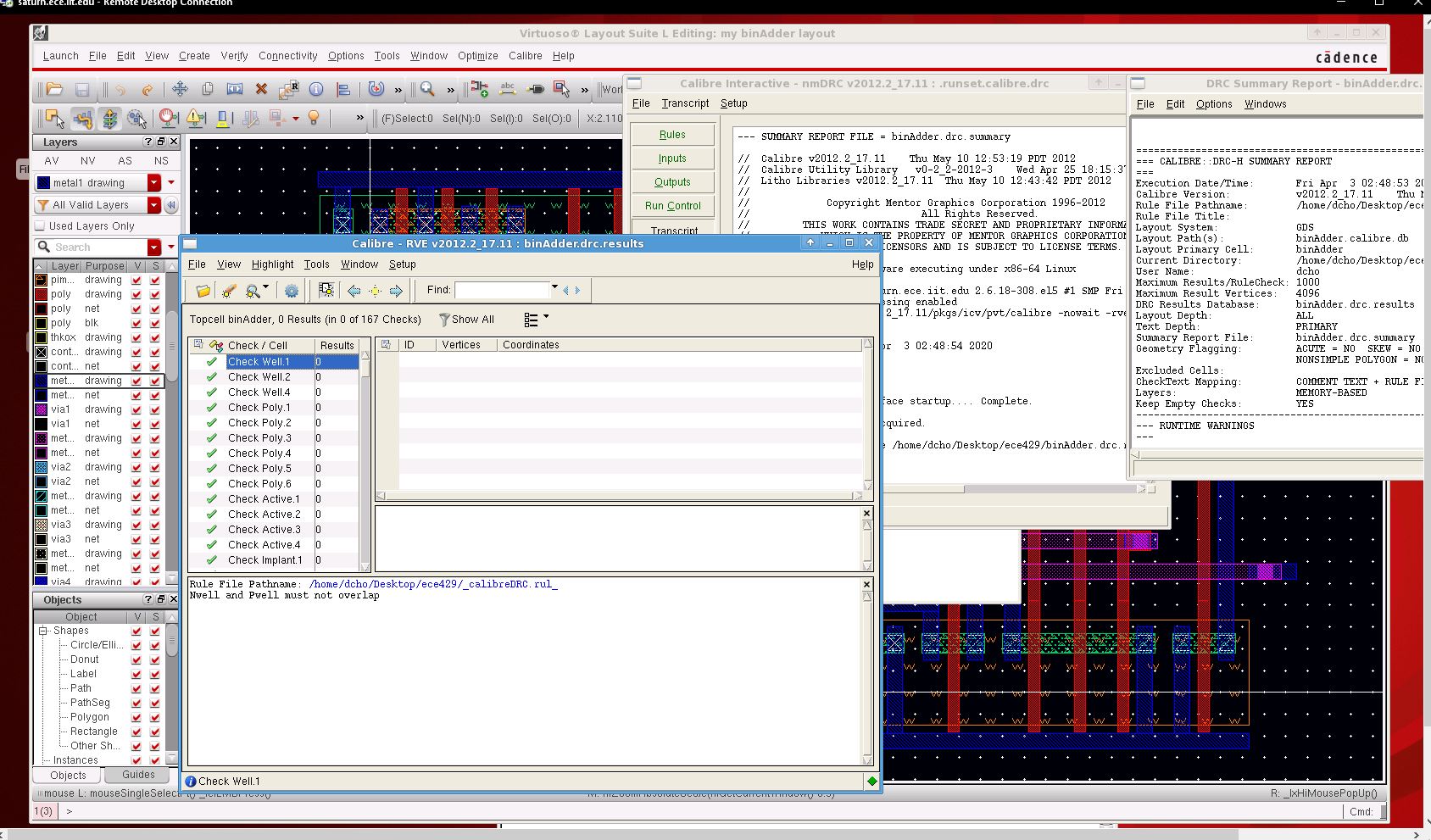
Using the example layout and the tutorial video, I made the layout

**Figure 2: Full-Adder Layout**

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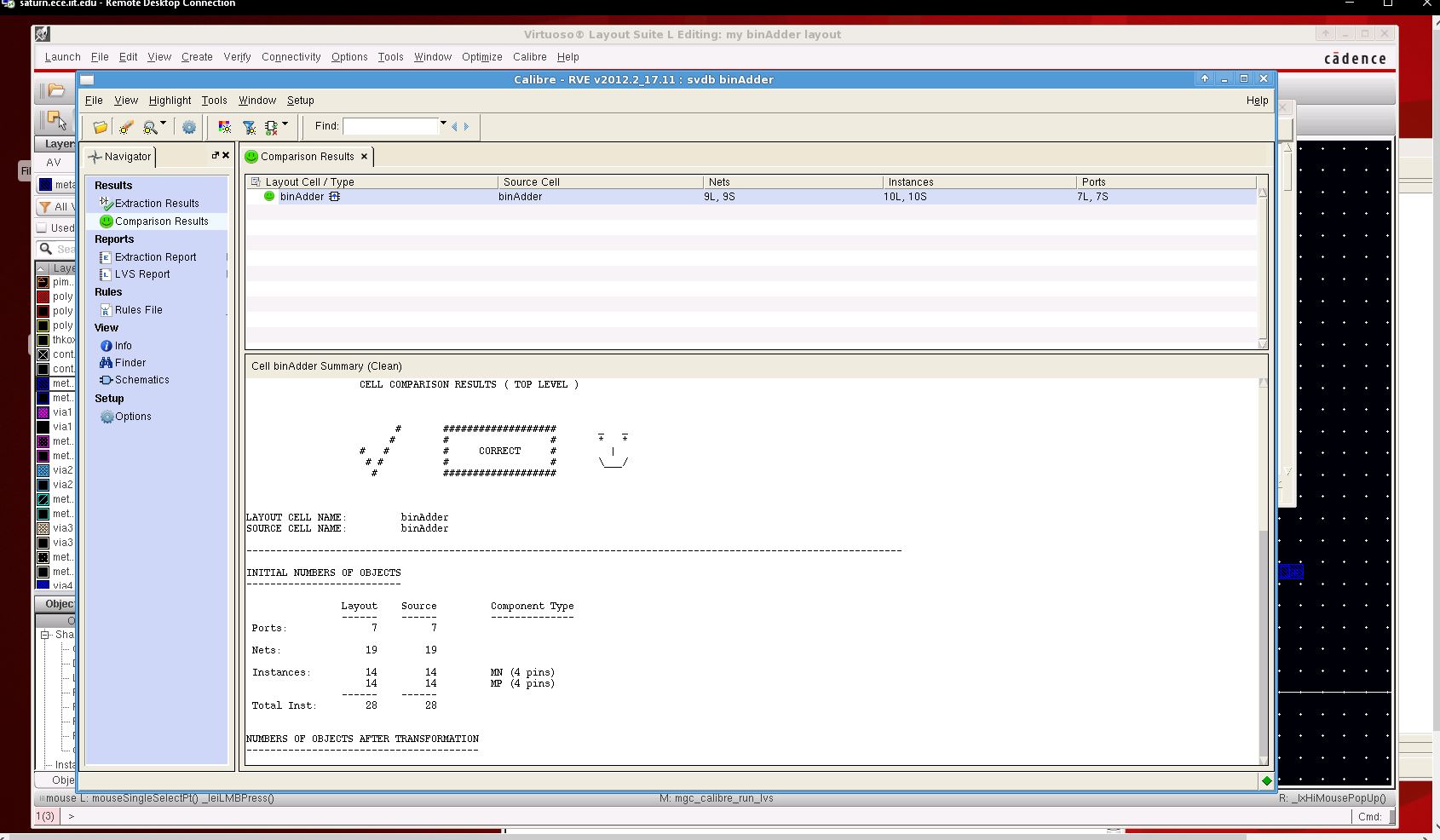
Throughout the process of designing the layout, a DRC was ran to check if the rules were being followed.

**Figure 3: DRC**

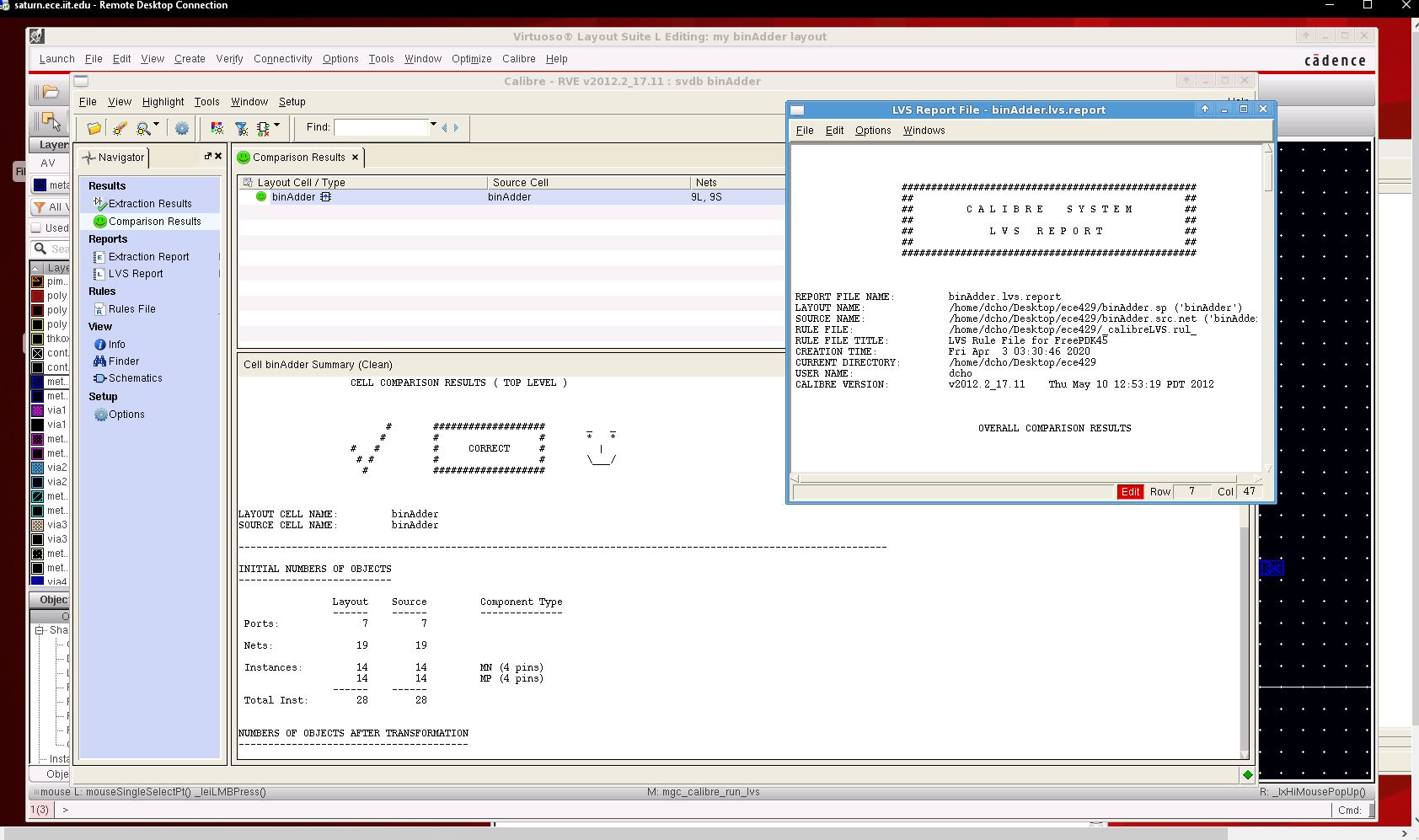
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After checking, I tested the LVS, which compares the layout to the schematic from the last lab. It took a long while to work out the kinks, but the LVS was eventually passed

**Figure 4: LVS Smile**

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**Figure 5: LVS Report**

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**Conclusion**

In conclusion, this was a successful lab. The layout for the full adder was successfully implemented and verified. Unfortunately, the lab was very time consuming. There were small details that got me tripped up and unable to finish the lab on time. I was eventually able to work out the small parts that I got wrong and pass the LVS.